WHAT IS CLAIMED IS:

1. A phase-change memory device, comprising:

a phase-change memory cell including a volume of material which is programmable between amorphous and crystalline states;

a write current source which selectively applies a first write current pulse to program the phase-change memory cell into the amorphous state and a second write current pulse to program the phase-change memory cell into the crystalline state; and

a restore circuit which selectively applies the first write current pulse to the phase-change memory cell to restore an amorphous state of the phase-change memory cell.

2. The phase-change memory device as claimed in claim 1, wherein the restore circuit further selectively applies the second write current pulse to the phase-change memory cell to restore a crystalline state of the phase-change memory cell.

3. The phase-change memory device as claimed in claim 1, further comprising a read circuit which reads the programmable state of the phase-change memory cell, wherein

the restore circuit is controlled by an output of the read circuit.

4. The phase-change memory device as claimed in claim 3, wherein the restore circuit is operable to apply the first write current pulse to the phase-change memory cell when the output of the read circuit indicates that the phase-change memory cell is in the amorphous state.

5. The phase-change memory device as claimed in claim 4, wherein the output of the read circuit is a global I/O line of the memory device.

6. The phase-change memory device as claimed in claim 4, wherein the output of the read circuit is a local I/O line of the phase-change memory device.

7. The phase-change memory device as claimed in claim 4, wherein the restore circuit further selectively applies the second write current pulse to the phase-change memory cell to restore a crystalline state of the phase-change memory cell.

8. The phase-change memory device as claimed in claim 1, wherein the volume of material is a chalcogenide alloy.

9. The phase-change memory device as claimed in claim 1, wherein the first write current pulse has an amperage which is greater than that of the second write current pulse, and wherein the first write current pulse has a pulse width which is less than that of the second write current pulse.

10. The phase-change memory device as claimed in claim 1, wherein the first write current pulse has an amperage which is the same as that of the second write current pulse, wherein the first write current pulse has a pulse width which is different than that of the second write current pulse, wherein the first write current pulse has a quenching time which is different than that of the second write current pulse.

11. The phase-change memory device as claimed in claim 1, wherein the memory device is switchable between a volatile mode and a non-volatile mode, and wherein the restore circuit is disabled during the non-volatile mode,

and wherein the restore circuit is enabled during the volatile mode.

12. A phase-change memory device, comprising:

a phase-change memory cell including a volume of material which is programmable between amorphous and crystalline states;

a write current source which operates in a low-power mode to selectively apply a first write current pulse to program the phase-change memory cell into the amorphous state and a second write current pulse to program the phase-change memory cell into the crystalline state, and which operates in a high-power mode to selectively apply a third write current pulse to program the phase-change memory cell into the amorphous state and a fourth write current pulse to program the phase-change memory cell into the crystalline state; and

a restore circuit which is operative in the low-power mode to selectively apply the first current pulse to the phase-change memory cell to restore an amorphous state of the phase-change memory cell.

13. The phase-change memory device as claimed in claim 12, wherein the restore circuit is further operative in the low-power mode to selectively apply the second write current pulse to the phase-change memory cell to restore a crystalline state of the phase-change memory cell.

14. The phase-change memory device as claimed in claim 12, wherein the low-power mode is a volatile mode of the memory device, and the high-power mode is a non-volatile mode of the memory device.

15. The phase-change memory device as claimed in claim 13, further comprising a read circuit which reads the programmable state of the phase-change memory cell, wherein the restore circuit is controlled by an output of the read circuit.

16. The phase-change memory device as claimed in claim 15, wherein the output of the read circuit is a global I/O line of the memory device.

17. The phase-change memory device as claimed in claim 15, wherein the output of the read circuit is a local I/O line of the phase-change memory device.

18. The phase-change memory device as claimed in claim 15, wherein the restore circuit is operable in the low-power mode to apply the first write current pulse to the phase-change memory cell when the output of the read circuit indicates that the phase-change memory cell is in the amorphous state.

19. The phase-change memory device as claimed in claim 18, wherein the restore circuit is further operative in the low-power mode to apply the second write current pulse to the phase-change memory cell when the output of the read circuit indicates that the phase-change memory cell is in the crystalline state.

20. The phase-change memory device as claimed in claim 12, wherein the volume of material is a chalcogenide alloy.

21. The phase-change memory device as claimed in claim 12, wherein the first write current pulse has an amperage which is greater than that of the second write current pulse, and wherein the first write current pulse has a pulse width which is less than that of the second write current pulse.

22. The phase-change memory device as claimed in claim 12, wherein the first write current pulse has an amperage which is the same as that of the second write current pulse, wherein the first write current pulse has a pulse width which is different than that of the second write current pulse, and wherein the first write current pulse has a quenching time which is different than that of the second write current pulse.

23. The phase-change memory device as claimed in claim 12, wherein an amperage of the third and fourth write current pulses are greater than the amperage of the first and second write current pulses.

24. A phase-change memory device which is operable in a non-volatile memory mode and a volatile memory mode, and

which comprises a phase-change memory cell including a volume of material which is programmable between amorphous and crystalline states, and a restore circuit which restores at least an amorphous state of the phase-change memory cell in the volatile memory mode.

25. A phase-change memory device as claimed in claim 24, wherein the restore circuit restores a crystalline state of the memory cell in the volatile memory mode.

26. A phase-change memory device as claimed in claim 24, wherein a state of the phase-change memory cell is not restored during the non-volatile memory mode.

27. A phase-change memory device as claimed in claim 24, wherein, when the volume of material is programmed in the amorphous state, less of the volume is amorphous in the volatile mode than in the non-volatile mode.

28. A phase-change memory device as claimed in claim 24, wherein, when the volume of material is programmed in the amorphous state, a degree to which a portion of the volume is amorphous in the non-volatile mode is greater

than a degree to which the same portion of the volume is amorphous in the volatile mode.

29. A phase-change memory device as claimed in claim 24, further comprising a read circuit which reads the state of the phase-change memory cell, wherein the restore circuit is controlled by an output of the read circuit.

30. The phase-change memory device as claimed in claim 29, wherein the restore circuit is operable to restore the amorphous state of the phase-change memory cell when the output of the read circuit indicates that the phase-change memory cell is in the amorphous state.

31. The phase-change memory device as claimed in claim 30, wherein the restore circuit is operable to restore the crystalline state of the phase-change memory cell when the output of the read circuit indicates that the phase-change memory cell is in the crystalline state.

32. The phase-change memory device as claimed in claim 29, wherein the output of the read circuit is a global I/O line of the memory device.

33. The phase-change memory device as claimed in claim 29, wherein the output of the read circuit is a local I/O line of the phase-change memory device.

34. The phase-change memory device as claimed in claim 24, wherein the volume of material is a chalcogenide alloy.

35. A phase-change memory device, comprising:

a data line;

a plurality of I/O lines;

a plurality of bit lines;

a plurality of word lines;

a plurality of phase-change memory cells at intersections of the word lines and bit lines, wherein each of said phase-change memory cells includes a volume of material which is programmable between amorphous and crystalline states;

a write current source which outputs first and second write current pulses to the bit lines according to a voltage of the data line, the first write current pulse for programming the phase-change memory cells into the

amorphous state and the second write current pulse for programming the phase-change memory cell into the crystalline state;

a plurality of sense amplifiers, respectively connected to the bit lines and the I/O lines, which read respective states of the phase-change memory cells; and

a restore circuit, connected to the I/O lines and to the data line, which controls the voltage of the data line to restore at least an amorphous state of the phase-change memory cells.

36. A phase-change memory device as claimed in claim 35, wherein the restore circuit further controls the voltage of the data line to restore a crystalline state of the phase-change memory cells.

37. The phase-change memory device of claim 35, wherein the memory device is switchable between a volatile mode and a non-volatile mode, and wherein the restore circuit is disabled during the non-volatile mode, and wherein the restore circuit is enabled during the volatile memory mode.

38. The phase-change memory device of claim 37, wherein the write current source outputs the first and second write current pulses to the bit lines in the volatile memory mode, and wherein the write current source further outputs third and fourth write current pulses in the non-volatile mode.

39. The phase-change memory device as claimed in claim 38, wherein the first write current pulse has an amperage which is greater than that of the second write current pulse, and wherein the first write current pulse has a pulse width which is less than that of the second write current pulse.

40. The phase-change memory device as claimed in claim 38, wherein the first write current pulse has an amperage which is the same as that of the second write current pulse, wherein the first write current pulse has a pulse width which is different than that of the second write current pulse, and wherein the first write current pulse has a quenching time which is different than that of the second write current pulse.

41. The phase-change memory device as claimed in claim 38, wherein an amperage of the third and fourth write current pulses are greater than the amperage of the first and second write current pulses.

42. The phase-change memory device as claimed in claim 35, wherein the volume of material of each of the phase-change memory cells is a chalcogenide alloy.

43. A method of programming a phase-change memory cell, the phase-change memory cell including a volume of material which is programmable between amorphous and crystalline states, said method comprising:

selectively applying first and second write current pulses to the phase-change memory cell, the first write current pulse for programming the phase-change memory cell into the amorphous state and the second write current pulse for programming the phase-change memory cell into the crystalline state;

detecting a state of the phase-change memory cell; and

conducting a first restore operation by again applying the first write current pulse to the phase-change memory

cell when the phase-change memory cell is detected as the amorphous state.

44. The method of claim 43, further comprising conducting a second restore operation by again applying the second write current pulse to the phase-change memory cell when the phase-change memory cell is detected as the crystalline state.

45. The method of claim 43, wherein the detection of the state of the phase-change memory cell occurs at each read operation of the phase-change memory cell, and wherein the first restore operation occurs at each read operation of the phase-change memory cell when the phase-change memory cell is detected as the amorphous state.

46. The method of claim 43, wherein the detection of the state of the phase-change memory cell occurs at each read operation of the phase-change memory cell, and wherein the first or second restore operation occurs at each read operation of the phase-change memory cell.

47. The method of claim 43, wherein the detection of the state of the phase-change memory cell repeatedly occurs at a regular interval, and wherein the first restore operation occurs at each regular interval when the phase-change memory cell is detected as the amorphous state.

48. The method of claim 47, wherein the regular interval is at least 60 minutes.

49. The method of claim 43, wherein the detection of the state of the phase-change memory cell repeatedly occurs at a regular interval, and wherein the first or second restore operation occurs at each regular interval.

50. The method of claim 49, wherein the regular interval is at least 60 minutes.